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(ii) forming a gate electrode layer on said gate insulating film. the gate electrode being retarded from edges of the gate insulating film, defining in each of the semiconductor layers a channel region below the gate electrode, and a pair of offset regions below the gate insulating film between the channel region and the end regions;

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(b) implanting dopant into the offset regions in each of said semiconductor layers through the gate insulation film by ion implantation to form lightly doped regions;

(c) implanting dopant into the end regions in each of said semiconductor layers directly to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions; and

(d) irradiating a laser beam directly or through said gate insulation film to said offset regions to activate dopants implanted in steps (b) and (c),

wherein said dopant cannot substantially be implanted into said offset regions.

REMARKS

As a preliminary matter, Applicant respectfully submits that the outstanding Office Action should be withdrawn as being not fully responsive. Specifically, the Examiner has stated on page 5 of Paper No. 18 that Applicant's arguments from Amendment C, filed January 9, 2002, "are moot in view of the new ground(s) of rejection." Contrary to this assertion, however, no new ground for rejection has been presented in Paper No. 18. In

Paper No. 18, the Examiner has merely cited Lee et al. (U.S. 5,677,206) as a new *reference*, and not as a new *ground* for rejection.

The Lee reference is only cited in the outstanding Office Action as cumulative support for the same grounds for rejection that stem from the Hodate et al. (U.S. 5,518,940) reference (which is again cited for these same grounds). The Examiner does not assert that Lee teaches or suggests anything new over Hodate, but only that Lee teaches the same features which Applicant had fully traversed in Amendment C. The specific grounds for traversal cannot be rebutted simply by presenting a redundant prior art reference, particularly when neither reference teaches or suggests all of the recited features of the claimed invention.

Furthermore, the Examiner even acknowledges that neither Lee nor Hodate show either of the patterned island-shaped semiconductor layers of the present invention, or the implantation of hydrogen in the present invention. Because such arguments were previously raised in Amendment C and left unrebutted, the addition of Lee to the outstanding Section 103 rejection does not, in fact, provide a new basis for rejection of the present invention, nor does it answer or rebut the arguments raised in Amendment C.

Furthermore, in the last Office Action (Paper No. 14), the Examiner cited only Yudasaka et al. (U.S. 5,563,427) as teaching island-patterned semiconductors and implanted hydrogen. As noted above, the Examiner admits Hodate (and similarly Lee) does not teach such features. In response, Amendment C included four pages of argument and discussion in

traversing the proposed combination, and the Yudasaka reference, as a basis for teaching or suggesting these features as in the present invention. These arguments have been left unrebutted by the Examiner, rendering the outstanding Office Action unresponsive. Yudasaka has again been presented as the only basis for teaching these features of the present invention.

Section 707.07(f) of the MPEP places the burden upon the Examiner to respond to each of the substantive arguments raised by Applicant in traversing the previous rejection, before repeating the rejection in a subsequent Action. The Examiner has not satisfied this burden which is required by the MPEP. Therefore, the outstanding Office Action should be vacated, and full consideration given to the arguments and discussion from Amendment C, particularly in regard to the Yudasaka reference.

In this light therefore, Applicant maintains and incorporates by reference herein those arguments previously advanced on pages 4-8 of Amendment C. Applicant respectfully requests that the Examiner reconsider those arguments, and withdraw the outstanding Section 103 rejection. Additionally, although Applicant does not agree that the Examiner's proposed combination is proper, nor admits that claims 1-6 and 22 read on the Examiner's proposed combination, Applicant has amended independent claims 1 and 22 only in order to expedite prosecution. In light of this amendment and the foregoing discussion, Applicant respectfully requests that the Examiner consider the following new arguments and comments expanding upon the previous arguments.

Claims 1-6 and 22 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Specifically, the Examiner has asserted that there is insufficient basis for the recited claim language "offset regions." Applicant respectfully traverses. Applicant points the Examiner's attention to page 13, lines 1-3 of the Specification to the present Application, where the formation and demarcation of "offset areas" are clearly disclosed. Moreover, FIG. 1A, as well as several subsequent drawings, all show these features of the present invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Claims 1-4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hodate or Lee, either taken with Yudasaka. Applicant again respectfully traverses this rejection as stated above, and because none of the cited references, whether taken alone or in combination, disclose or suggest the offset regions of the present invention, or that hydrogen ions are not implanted in the channel region under the gate electrode, as featured in the present invention.

As acknowledged by the Examiner, neither Hodate nor Lee disclose or suggest a semiconductor island, implanted hydrogen, or a channel region beneath the gate electrode where no hydrogen is implanted. Only Yudasaka has been cited for teaching such features. However, Yudasaka does not disclose features analogous to those in the present invention.

None of the three cited references disclose or suggest offset regions or a gate insulating film formed between the substrate and the gate electrode layer, as in the present

invention. As can be seen in FIG. 1A of the present invention, for example, an island-shaped polysilicon layer 4 is formed on a substrate 1. A gate insulating film 6 is formed on top of the layer 4, but only partially covers the layer 4. A gate electrode 8 is formed on top of the insulating film 6, but similarly only covers a portion of the film 6. The channel region and offset regions in the layer 4 are thus defined by the dimensions of the partial coverage of the insulating film 6 and gate electrode 8 over the layer 4. Such a structural configuration is neither disclosed nor suggested by Yudasaka, or in any of the cited references.

Both Yudasaka and Hodate show a gate insulating film between a semiconductor and a gate electrode. However, referring to FIG. 4 of Yudasaka, Yudasaka specifically discloses that the gate insulating film 124, which lies beneath the gate electrode 125, entirely covers the surface of the island-shaped semiconductor 121-123. Because this gate insulating film according to Yudasaka always covers the entire semiconductor, no corresponding channel region, offset regions, or outer regions could be formed and defined as they are in the present invention.

The Examiner asserts that Hodate on the other hand, shows such offset regions in FIGs. 4B and 4C. However, contrary to the Examiner's assertion, the indicated regions 18 of Hodate are not analogous to the offset regions of the present invention. Similar to Yudasaka, Hodate discloses a gate insulating film 3 between the region 18 and the gate electrode 4. But also similar to Yudasaka, the gate insulating film 3 is shown to cover the entire area above the region 18, as well as additional outer regions 20 and 21. Hodate further

discloses a pair of heavily doped regions source/drain regions 48 separated from the channel region 44. (See FIGS. 8A-8C). The separation is defined by the outer dimensions of the resist film 47. Again though, no offset regions, as in the present invention, are shown.

The offset regions of the present invention therefore can not be suggested by Hodate, Lee, or Yudasaka. Independent claims 1 and 22 have been amended to even further clarify the differences between the present invention and the prior art. The claims now clearly feature that the gate insulating film forms wing-like portions outside the gate electrode defining the lightly doped offset regions. The exposed semiconductor regions outside the offset region "wings" will thus become heavily doped source/drain regions. The channel region under the gate electrode is defined to contain no hydrogen implantation. This configuration is not taught or suggested by any combination of the cited prior art references. Accordingly, for at least these reasons, the Section 103 rejection based on combinations of Hodate, Lee, and Yudasaka is respectfully traversed.

Furthermore, as discussed above, none of the cited references teach or suggest a channel region under the gate electrode where no hydrogen is implanted. The present invention, on the other hand, does feature a channel region beneath the gate electrode with no implanted hydrogen. Yudasaka, for example, teaches a channel region, but remains silent as to whether hydrogen is implanted into the channel region.

As disclosed on page 9 of the Specification to the present Application, implanted hydrogen is known to pass through the gate electrode and be undesirably

distributed widely in the layers beneath the gate electrode. The present invention, however, solves this problem and prevents implantation of hydrogen into the channel region beneath the gate electrode. A problem faced and solved by the present inventor should be considered before making a determination based on obviousness.

Unlike the present invention, Yudasaka is silent regarding the problem of hydrogen implantation beneath the gate electrode. In fact, as the only reference cited for even teaching hydrogen implantation, Yudasaka does not even suggest that such a problem exists. Furthermore, the arguments for why Yudasaka would actually include hydrogen in the channel region were discussed in detail in Amendment C, and incorporated by reference into this Amendment. To date, these arguments remain unrebutted by the Examiner. For at least these additional reasons therefore, the present invention is distinct from all three of the cited references of record, and the Section 103 rejection is again respectfully traversed.

Additionally, because none of the three cited references even addresses the problem of limiting the implantation of hydrogen into the layers beneath the gate electrode, the present invention is nonobvious over the proposed combination. Only Yudasaka of the three references even briefly mentions hydrogen implantation. However, Yudasaka fails to mention or address any of the problems associated with hydrogen implantation.

To maintain a rejection based on obviousness, there must be some teaching or suggestion within the prior art to actually combine the teachings of the references. Without such a suggestion for the *combination*, such a combination would not be obvious without the

benefit of the present inventor's own Application. Such is the case here. There can be no suggestion from any of the three references to combine the teachings of these references to limit the implantation of hydrogen in the layers beneath the gate electrode because none of the three references even recognizes or suggests such a need. Accordingly, for these reasons as well, the Section 103 rejection based on a combination of Hodate, Lee, and Yudasaka is further traversed.

In addition to the clarifying amendments discussed above, the Specification has been also been amended to correct a spelling error. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment. The attached Appendix is captioned "**Version with Markings to Show Changes Made**."

Accordingly, for all the foregoing reasons, Applicant submits that this Application, including claims 1-6 and 22, is in condition for allowance, which is once again respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the paragraph beginning on page 3, line 19 as follows:

FIG. 2A shows a first TFT structure. In the first structure, an island-shaped polysilicon layer 204 is formed on a [grass] glass substrate 201, and a gate insulation film 206 is formed on the [grass] glass substrate 201 so as to cover the polysilicon layer 204. A gate electrode 208 is formed on the gate insulation film 206 so as to be just above a central portion of the island-shaped polysilicon layer 204.

IN THE CLAIMS:

Claims 1 and 22 have been amended as follows:

1. (Four Times Amended) A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on and across an intermediate region of each of the semiconductor layers the gate insulating film having a thickness not larger than 50 nm, and exposing end regions of each of the semiconductor layers;

(ii) forming a gate electrode on the gate insulating film over each of said semiconductor layers, the gate electrode being retarded from edges of the gate insulating film, defining in each of the semiconductor layers a channel region below the gate electrode, and a pair of offset regions below the gate insulating film between the channel region and the end regions;

(b) implanting dopant into [first regions at outsides of regions designated for offset regions adjacent to a channel region under said gate electrode] the offset regions in each of said semiconductor layers [directly or] through [a thin] the gate insulation film [whose thickness is equal to or less than 50nm] by ion implantation to form lightly doped regions; and

(c) implanting dopant into [outer] the end regions [within said first regions] in each of said semiconductor layers directly [or through said thin insulation film] to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions,

wherein said ion implanting steps (b) and (c) are so selected that hydrogen ions are also implanted into said lightly doped regions and said heavily doped source/drain regions, but not into said channel region under said gate electrode, and

wherein said dopant cannot substantially be implanted into said offset regions.

22. (Twice Amended) A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on and across an intermediate region of said substrate, said film covering at least a portion of said semiconductor layers, the gate insulating film having a thickness not larger than 50 nm, and exposing end regions of each of the semiconductor layers;

(ii) forming a gate electrode layer on said gate insulating film, the gate electrode being retarded from edges of the gate insulating film, defining in each of the semiconductor layers a channel region below the gate electrode, and a pair of offset regions below the gate insulating film between the channel region and the end regions;

(b) implanting dopant into [first regions at outsides of regions designated for offset regions adjacent to a channel region] the offset regions in each of said semiconductor layers [directly or] through [a thin] the gate insulation film [whose thickness is equal to or less than 50nm] by ion implantation to form lightly doped regions;

(c) implanting dopant into [outer] the end regions [within said first regions] in each of said semiconductor layers directly [or through said thin insulation film] to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions; and

(d) irradiating a laser beam directly or through said [thin] gate insulation film to said [first] offset regions to activate dopants implanted in steps (b) and (c),

wherein said dopant cannot substantially be implanted into said offset regions.